Claims

1. A high density memory card comprising:
a module card on which there are assembled a plurality of dual device stacks each having a center bus wire, said plurality of dual device stacks including:
a first lower layer memory device attached to a substrate, said substrate having a plurality of wire bond pads adjacent to an aperture in said substrate center for connection to said center bus wire; and
a first upper layer memory device stacked on top of said first lower layer memory device such that said first upper layer memory device is offset over said first lower layer memory device exposing said center bus wire of said first upper layer memory device to some of said plurality of wire bond pads at an edge of said first lower layer memory device;
said center bus wire of said upper layer memory device connected to said wire bond pads of said substrate around said edge of said first lower layer memory device.

2. The memory card of claim 1 including said substrate having apertures therethrough such that said center bus wire of said upper layer memory device traverses through said aperture to said wire bond pads on the opposite side of said substrate from that which said lower layer memory device is bonded.

3. The memory card of claim 1 further including said dual device stacks placed adjacent to one another in a line.

4. The memory card of claim 3 wherein said dual device stacks are placed in an array comprising rows and columns.

5. The memory card of claim 1 wherein said offset further includes placing an end of an upper layer memory device of a first dual device stack at approximately the center of a lower layer memory device of a second dual device stack.

6. The memory card of claim 1 wherein said lower layer memory device attaches to said module card via ball grid arrays.

7. A substrate having wire bond pads and a plurality of memory devices with center bus wires attached thereto, said substrate comprising:
a first layer of said plurality of memory devices attached to said wire bond pads, adjusted such that a gap exists between adjacent first layer memory devices; and
a second layer of said plurality of memory devices, each second layer device bonded to and on top of a first layer device such that said center bus wire of said second layer device traverses through said gap to said wire bond pads.

8. The substrate of claim 7 further comprising said substrate having apertures therethrough such that said center bus wires of said second layer devices traverse through said apertures to wire bond pads on the opposite side of said substrate from that which said first layer memory devices are bonded.

9. The substrate of claim 7 wherein each of second layer devices is offset from said first layer devices underneath by approximately a device width, such that each of said second layer devices is centered with respect to said gaps.

10. A method of assembling memory devices having center bus wires, said method comprising:
providing a substrate having a top and bottom surface with wire bond pads for electrical connection;
bonding a first dual device stack of memory devices having an upper memory device and a lower memory device to said wire bonds on said top surface of said substrate, said lower memory device placed adjacent to a lower memory device of a second dual device stack of memory devices, with gaps therebetween; and

bonding a second dual device stack of memory devices to said first dual device stack of memory devices such that an upper memory device in said second dual device stack of memory devices is offset over said gap with said center bus wires traversing therethrough.

11. The method of claim 10 further comprising having said center bus wire of said upper memory device traverse through an aperture in said substrate to electrically connect with said wire bond pads on said substrate's bottom side.

12. The method of claim 10 including having said offset adjusted for approximately centering each of said upper memory devices of said dual device stack of memory devices over two adjacent lower memory devices of said dual device stack of memory devices.

13. The method of claim 10 including placing said dual device stacks of memory devices adjacent to one another in a line.

14. The method of claim 13 wherein placing said dual device stacks of memory devices includes forming an array of said dual device stacks of memory devices comprising rows and columns.

15. The method of claim 10 including encapsulating some of said dual device stacks in resin on a portion of surfaces or all surfaces.